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Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Conceptual Design of the Glast Calorimeter Readout Control (GCRC) ASIC

(Concept stage, Ver 2)

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1 PURPOSE

This document describes the conceptual design for the GLAST Large Area Telescope (LAT) Calorimeter Readout control (GCRC) ASIC.

2 SCOPE

This document gives an overview over the conceptual architecture of the GLAST LAT Calorimeter Readout Control (GCRC) ASIC.

3 DEFINITIONS

3.1 Acronyms

GLAST – Gamma-ray Large Area Space Telescope

GCFE – Glast Calorimeter Front-end Electronics

GCRC – Glast Calorimeter Readout Control electronics

GRB – Gamma-Ray Burst

LAT – Large Area Telescope

TBR – To Be Resolved

CAL – Calorimeter Detector

L1_TACK – Level 1 Trigger Request

L1_TREQ – Level 1 Trigger Request

GLB-TRG – Global L1 Trigger

TEM – Tower Electronics Module

3.2 Definitions

μ sec, μ s – Microsecond, 10^{-6} second

Dead Time – Time during which the instrument does not sense and/or record gamma ray events during normal operations..

s, sec – seconds

4 APPLICABLE DOCUMENTS

Documents that are relevant to the development of the GCFE concept and its requirements include the following:

4.1 Requirement Documents

GLAST00010, “GLAST Science Requirements Document”, P.Michelson and N.Gehrels, eds., July 9, 1999.

LAT-SP-00010, “GLAST LAT Performance Specification”, August 2000

LAT-SS-00018, “LAT CAL Subsystem Specification”, January 2001

4.2 Conceptual Design Documents

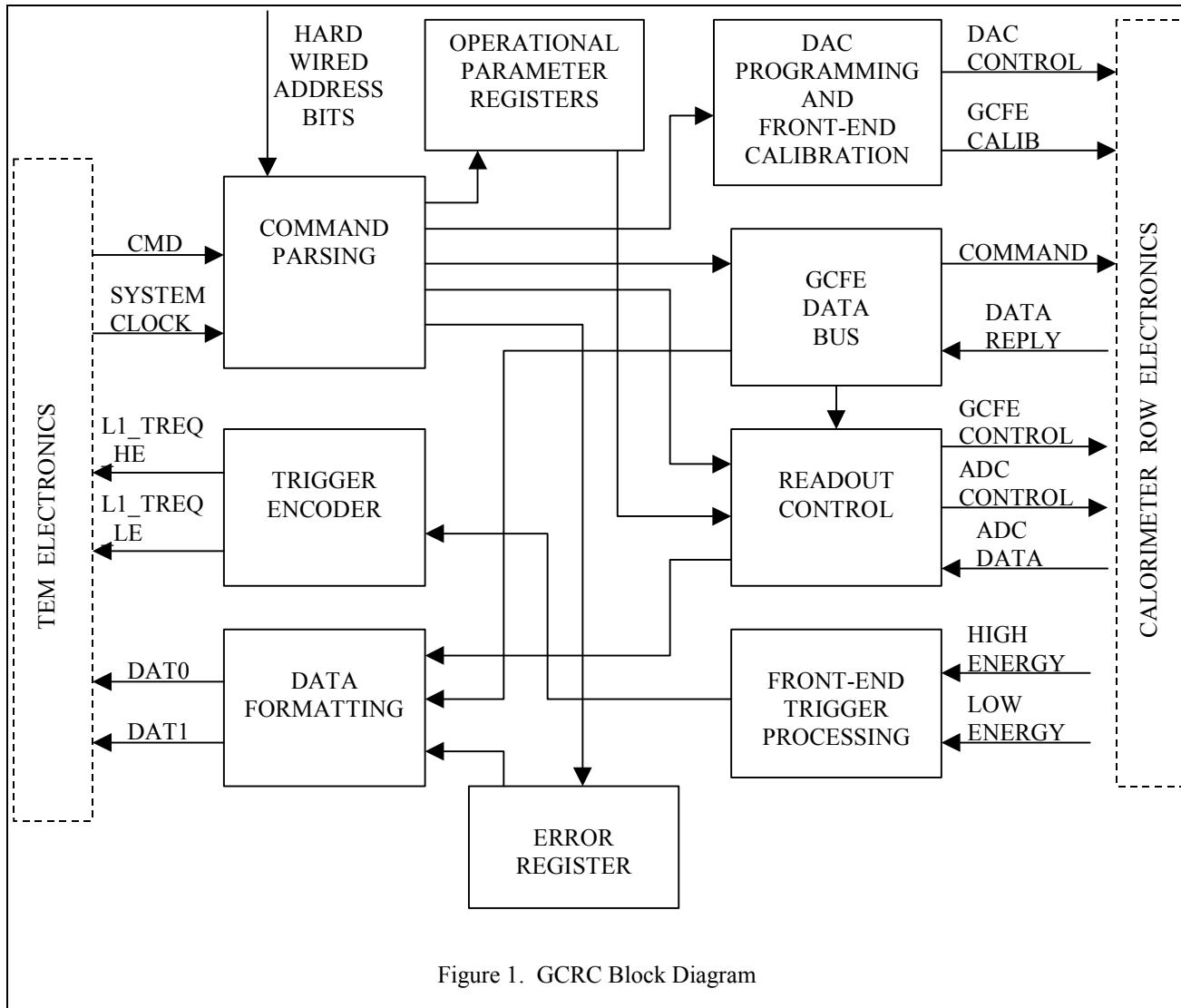
- [1] GLAST Calorimeter Analog Front-End ASIC Design Consideration, Neil Johnson, NRL
- [2] Conceptual Design of the GLAST Calorimeter Front End ASIC, Gunther Haller
- [3] LAT Electronics System – Conceptual Design
- [4] LAT Calorimeter Electronics System
- [5] LAT GCFE Specification
- [6] LAT TKR-CAL Tower Electronics Module – Conceptual Design
- [7] LAT Control Protocol within LAT – Conceptual Design
- [8] LAT Data Protocol within LAT – Conceptual Design
- [9] LAT Housekeeping within LAT – Conceptual Design
- [10] LAT L1 Trigger System – Conceptual Design

5 INTRODUCTION

The *GLAST* electronics system is described in [3]. The calorimeter sub-system electronics is documented in [4]. One of the two custom ASICs required is the Glast Calorimeter Readout Control (GCRC) Application Specific Integrated Circuit (ASIC). The basic function of the GCRC is the interface between the Tower Electronics Module (TEM) and the Glast Calorimeter Front End (GCFE). ASIC The GCRC passes commands from the TEM to GCFEs, controls event readout of the log ends, and passes data back to the TEM. The GCRC is a digital chip with Low Voltage Differential Signalling (LVDS) Inputs and Outputs (I/O). Target fabrication processes for the ASIC are the 0.5 um Agilent CMOS and the 0.5 um Peregrine SOI.

The GCRC described in this document serves one calorimeter layer. There are four layers per calorimeter side.

The conceptual design in this document is based on interfaces required between the GCFE design documented in [3] and the TEM design documented in [6].



6 GCRC Description

6.1 GCRC Overview

The GCRC ASICs are the interface between the 192 log-end GCFE ASICS and the single TEM, per tower module. The functionality of the GCRC is partitioned such that one GCRC ASIC interfaces one layer, 12 log ends, of the calorimeter. This calorimeter row partitioning follows from using “wired-OR” triggering per calorimeter row and calorimeter printed circuit board constraints of more horizontal routing space than vertical. The GCRCs receive a constant 20 MHz system clock from the TEM, the same clocking frequency of all communication with the TEM.

6.2 Command Parsing

Figure 1 includes a block for parsing of commands from the TEM. The TEM to GCRC command lines are bussed in parallel to all four GCFE ASICS per side of the calorimeter, refer to Figure 2.

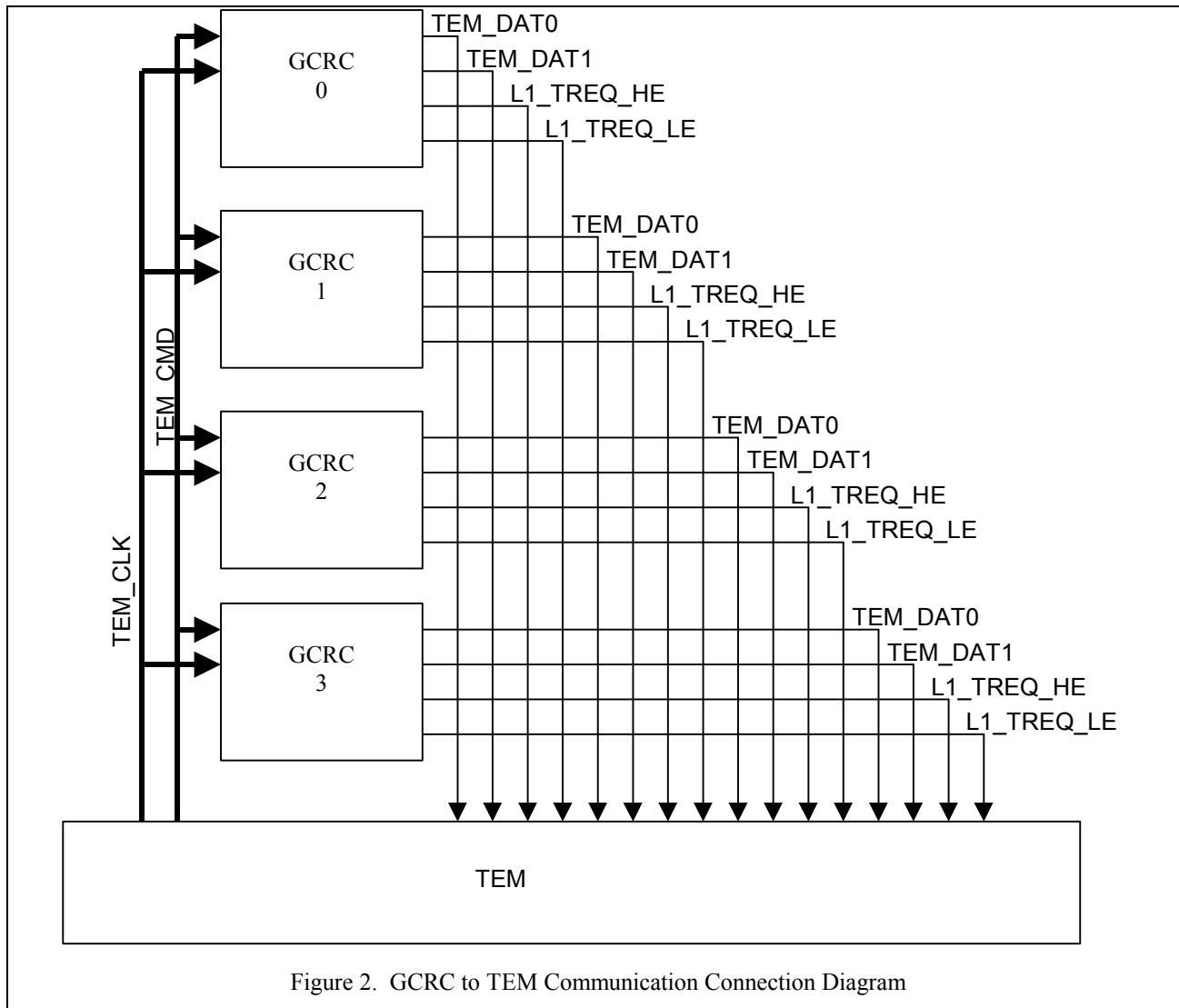


Figure 2. GCRC to TEM Communication Connection Diagram

The TEM Command is one of three types:

- Command Signal Readout (Trigger)
- Command Register Load
- Command Register Read

The first two bits in the TEM_CMD line following the start bit indicates a Signal Readout command or Register Load/Read operation. If the two Readout bits are asserted, then the command is for a Signal Readout (Trigger), and the next four bits determine the signal readout type. See Figure 3 for timing diagram Table 1 for Bit definitions.

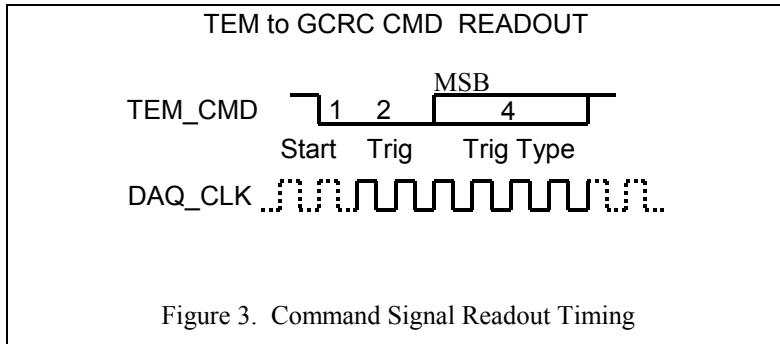
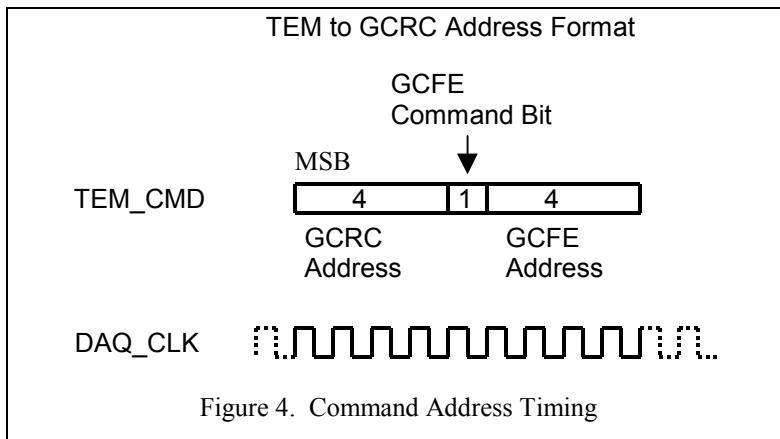


Table 1. Trigger Type Bit Definitions

Bit	Definition
0 LSB	4 Range Readout
1	4 Range Readout
2	Always 0
3 MSB	Always 0

The Register Read/Load commands are either directed to a particular GCRC (row), particular GCFE (log end), or broadcast to all devices ‘listening’. Register operations are initiated from the TEM by two not-asserted Signal Readout bits following the start bit. An address follows which generally points to a specific GCRC or GCFE device. A GCFE Command Bit bit is included in the address to indicate whether the command is directed to a GCFE device, bit asserted, or GCRC device, bit unasserted. See Figure 4.



To facilitate device addressing, each of the four GCRCs per calorimeter side and each of the 12 GCFE’s per row has a unique hard-wired address for decoding the command address bits.

Upon a GCRC chip decoding a command with GCRC address matching its wired address, and the Address/Function parity checks good, the GCRC has two options:

- a) GCFE Command Bit not asserted: Decode function bits at the GCRC and act upon command See Figure 5 and Figure 6

b) GCFE Command Bit asserted: forward command to GCFE's on row stripped of GCRC address and parity bits. See Figure 7 and Figure 8.

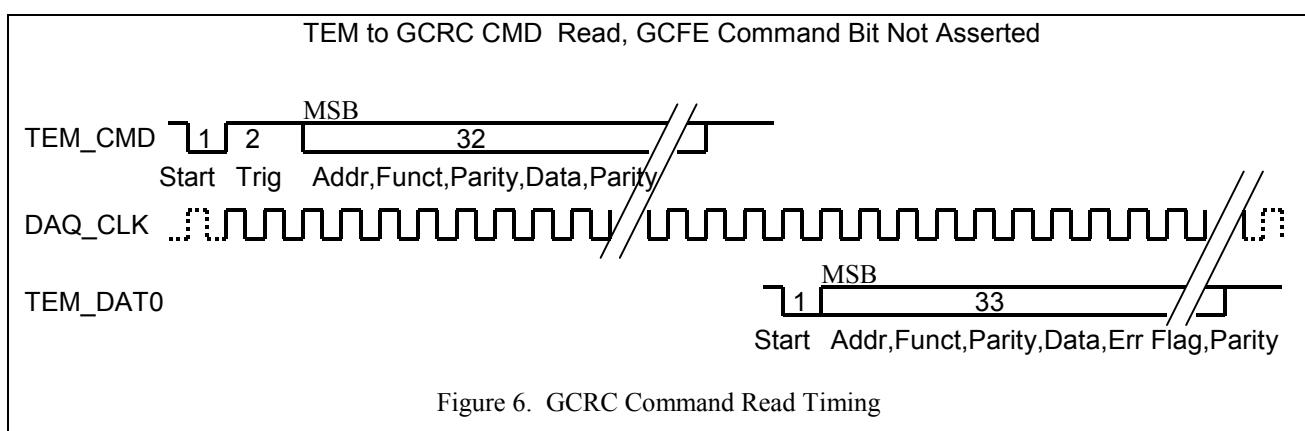
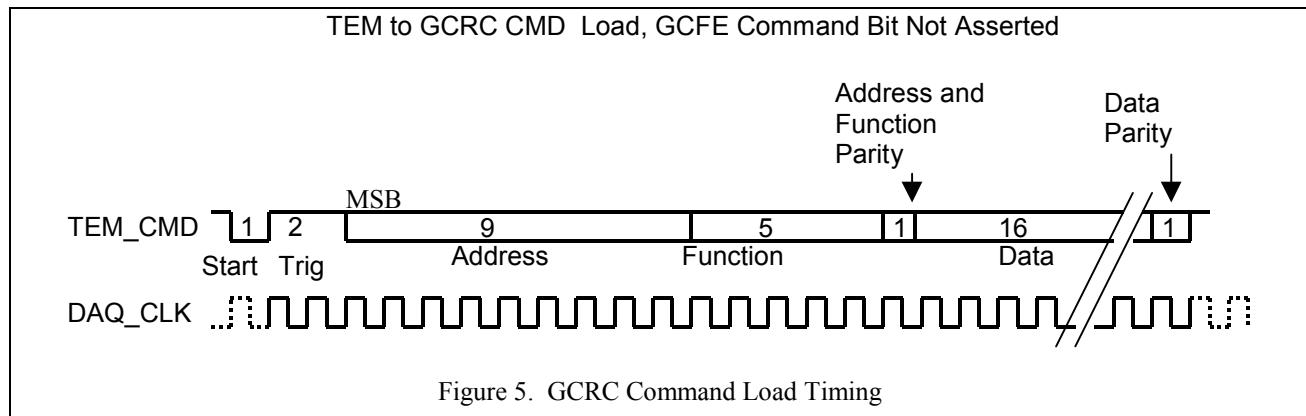


Figure 5 shows the command structure to load a GCRC register. Figure 6 shows the structure for GCRC register read. The returned address and function bits are repeated from the command. The Parity bits are recomputed, according to the parity type set in the GCRC configuration register, Table 3. The returned data parity is computed on the returned data and Error Flag bit.

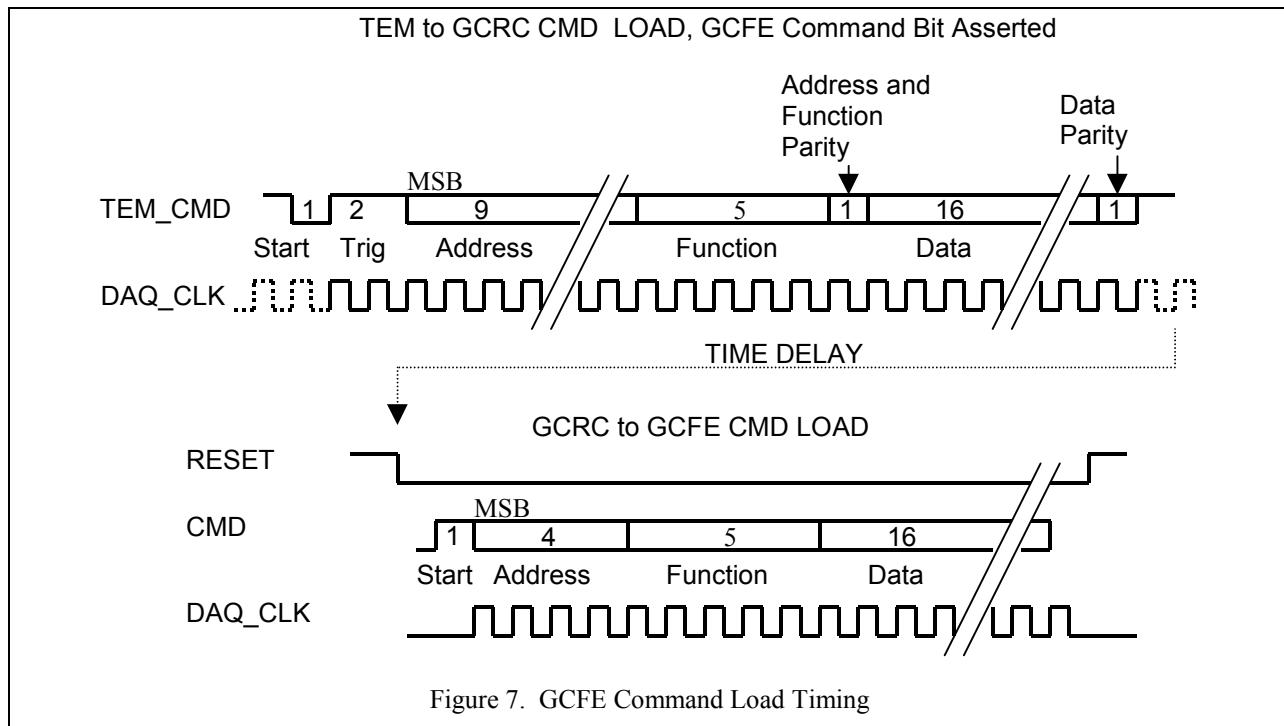


Figure 7 shows the command structure for a GCFE Load command. Note that the GCRC forwards the command stripped of the GCRC address and parity bits. Also, the command is only forwarded after all parity bits check correctly.

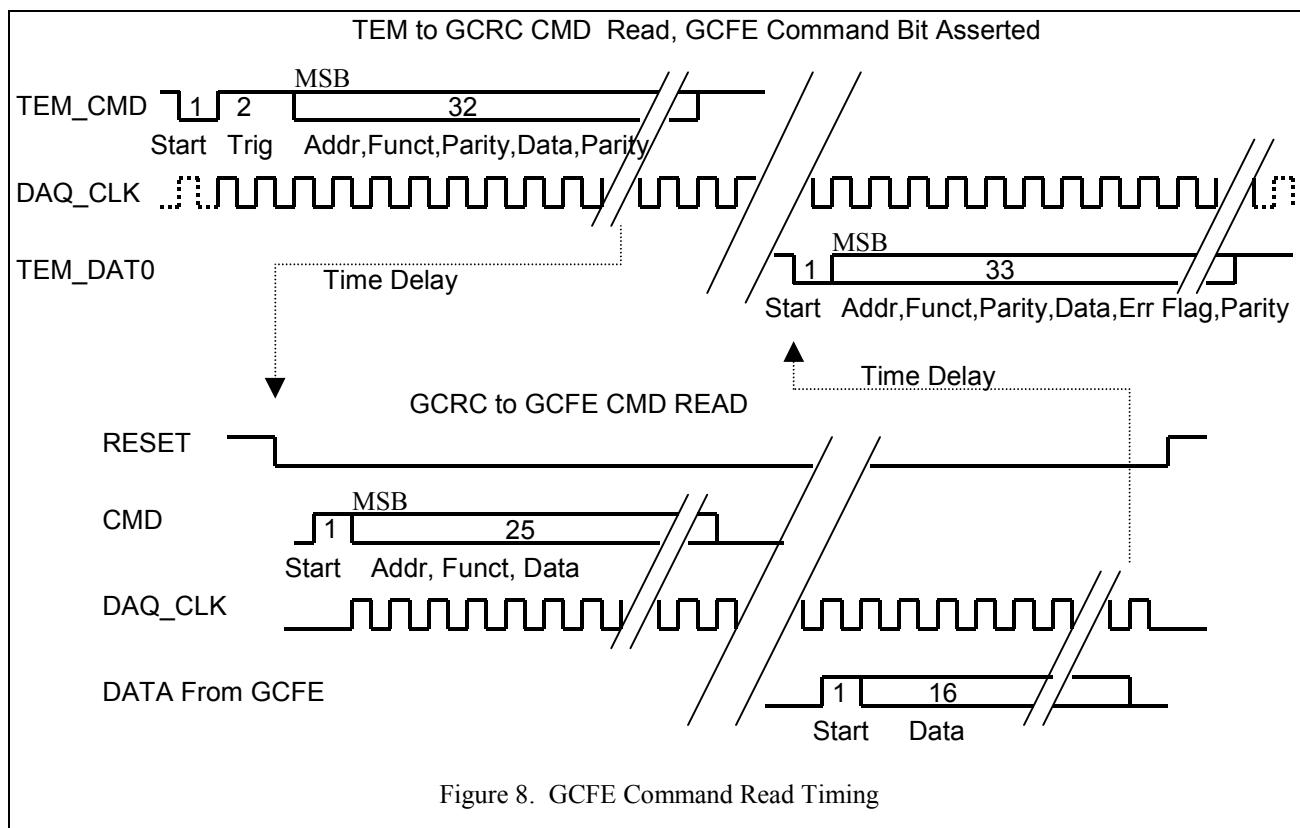


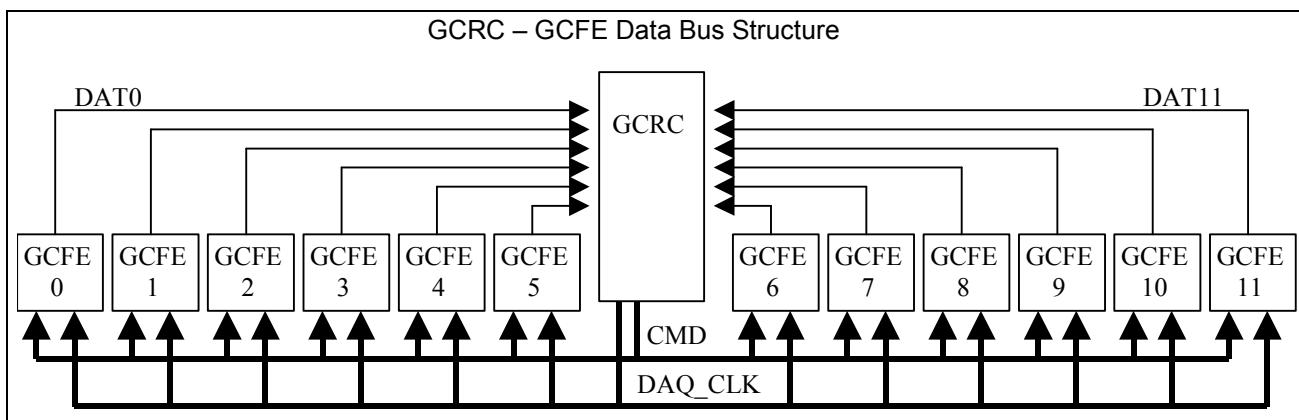
Figure 8 shows the command structure for GCFE Read command. Note again that the GCRC forwards the command stripped of the GCRC address and parity bits. Since no useful data is sent to the GCFE with a read command, the command can be sent to the GCFE following the Address/Function parity bit checking correctly. The reply to the TEM is rebuilt using the original address and function bits from the command, with parity recomputed according to the GCRC configuration register. The returned data is that data returned from the GCFE chip addressed in the command. The data parity is computed on the returned data and Error Flag bit, parity format according to the GCRC configuration register.

If there are any errors in the described processes, the first 16 bits of the received command is saved in a error register and a global GCRC error flag is set. The error flag status is sent back to the TEM at the end of the next read command. The error flag is reset following transmission of its status.

Communication with the TEM on the TEM_CMD line and the TEM_DAT0 line is done with Low Voltage Differential Signalling (LVDS) asserted low.

6.3 GCFE Data Bus

The GCRC log-end commands are bussed in parallel to the GCFE chips. The 12 GCFE chips per GCRC have four uniquely hard-wired address lines to decode the addressed command. The commands to the GCFE chips use LVDS lines. The GCRC receives reply data back through individual LVDS data lines from each GCFE chip.



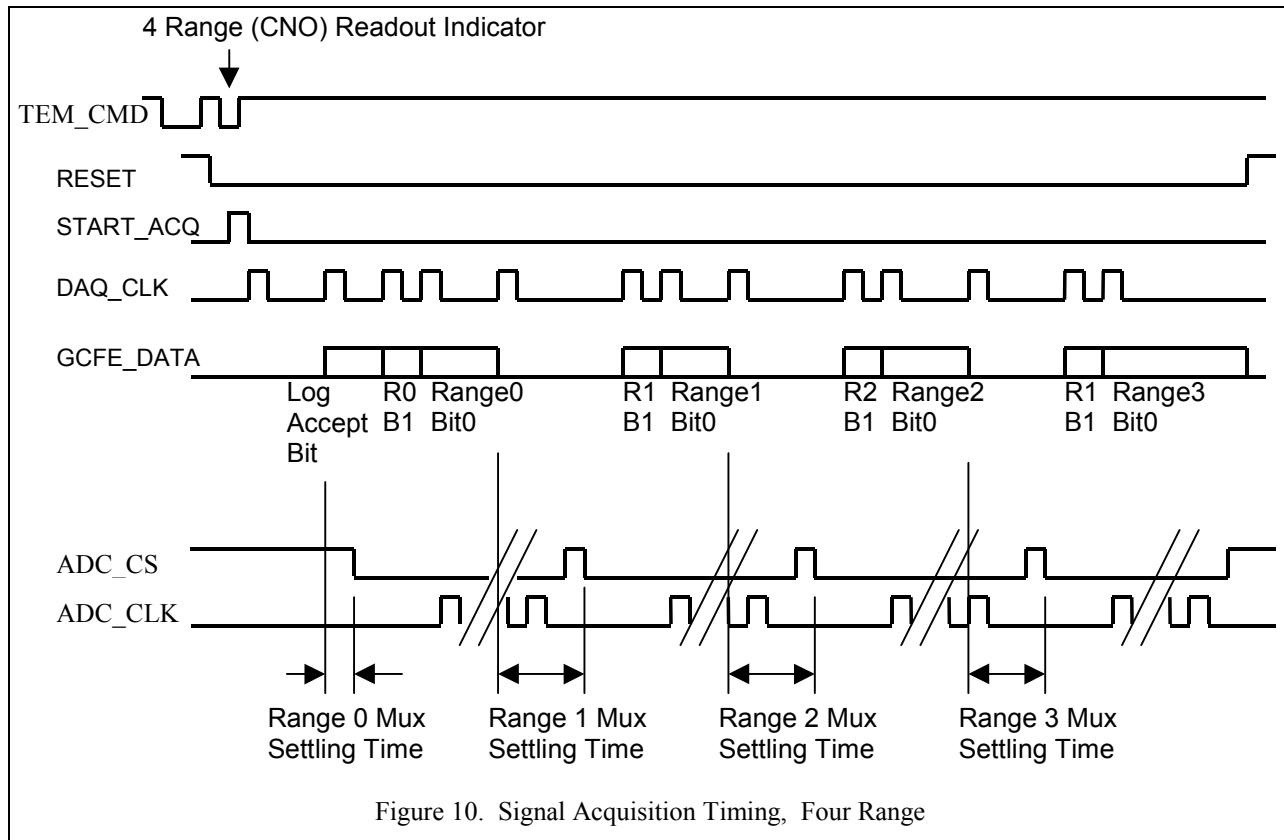
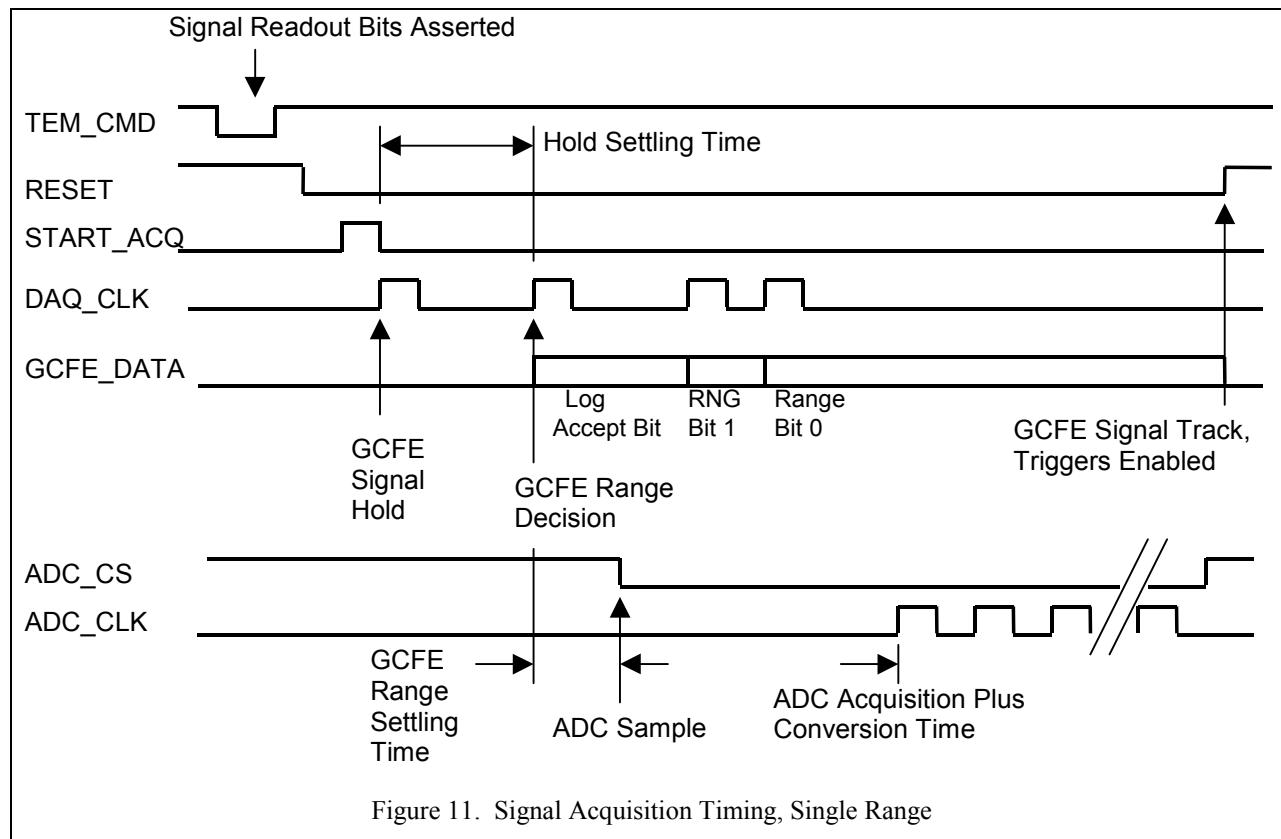
6.4 Readout Control

Upon receiving a Signal Readout (trigger) command, the GCRC immediately executes a readout cycle by directing the GCFE chips through the signal acquisition cycle, and controlling the digitization by the ADCs. Refer to Figure 11.

The nominal readout is digitization of one of the four possible GCFE ranges. Additionally, GCRC can be directed, through the TEM_CMD line to digitize all four GCFE ranges, as shown in Figure 10.

Through prior TEM commanding, each GCFE chip is nominally allowed to decide its own optimum range to readout per event. Thus for correct association of the ADC data, the GCRC readout control reads two range definition data bits from each GCFE chip, per range digitized. The range definition bits are passed with the ADC data to the TEM.

Zero suppression, the process of discarding minimal amplitude data, is made easier with a dedicated discriminator bit in each GCFE chip. The GCRC reads this bit, termed 'Log-Accept Bit', from each GCFE chip during the first range readout cycle. This bit is again passed with the ADC data, enabling the TEM to quickly zero suppress data with no computation.



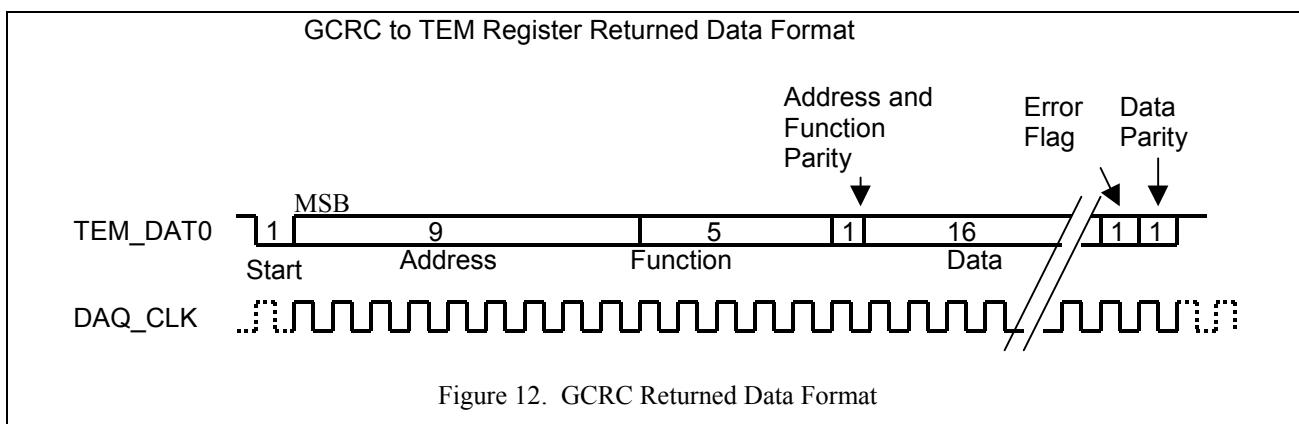
6.5 Data Formatting

Data sent to the TEM is of two varieties:

- a) Register data following a Read Register command
- b) Log-end digitized data following a Signal Readout command.

There is no indicator in the bitstream for the two varieties of data. But since both are returned from TEM commands, the TEM knows which type of data is returned.

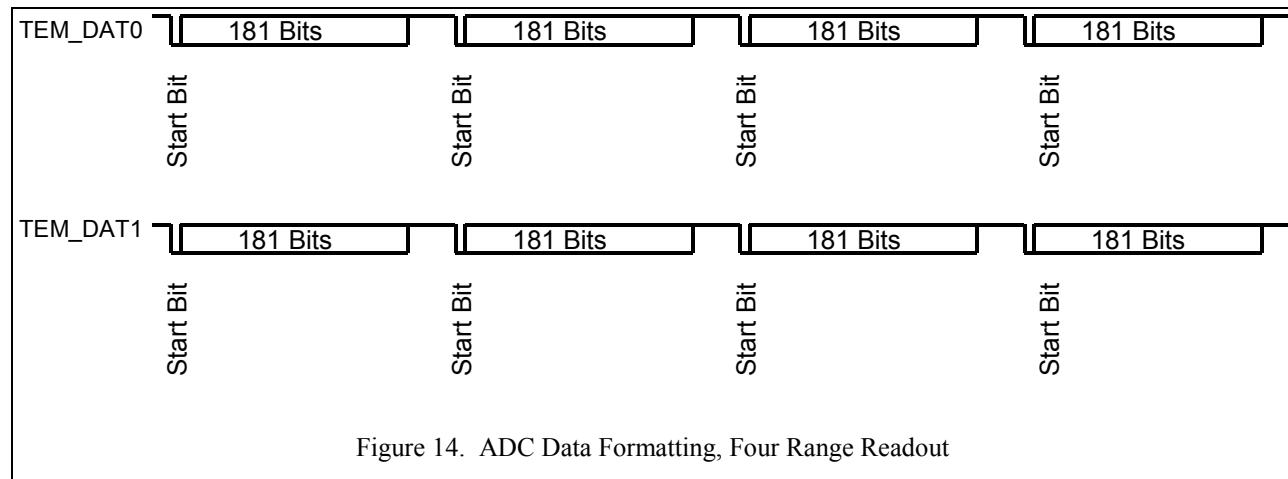
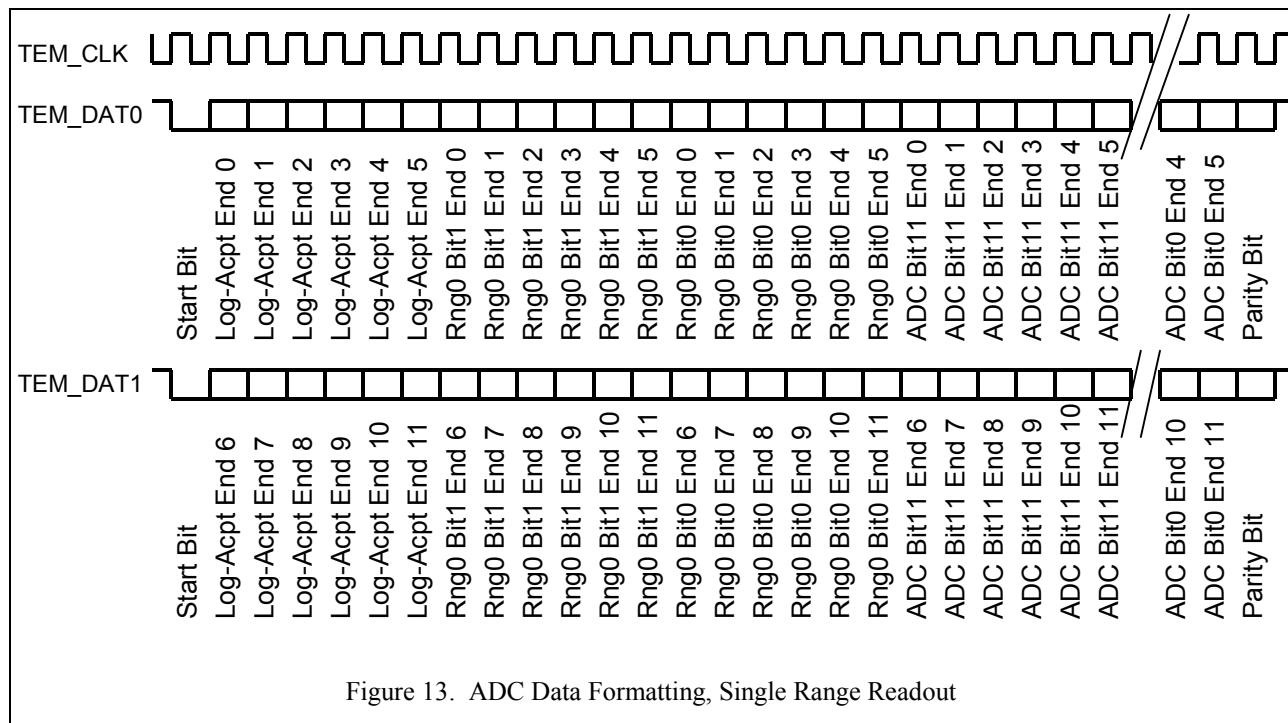
For register data, the returned data format is shown in Figure 12.



The Address and Function bits are repeated from the initiating command. The Address/Function parity bit is recomputed in accordance to the parity selected in the GCRC configuration register. The data is returned is a copy from the register selected. The error flag is asserted if there has been any type of error in the GCRC commanding. The error flag register is cleared following transmission.

For Signal Readout data, the format is shown in Figure 13 for single range readout and Figure 14 for four range readout. The GCFE range bits and zero suppression bits are sent to the TEM ahead of the ADC data, with ordering similar to that of the ADC bits. The ADC bits are sent to the TEM without grouping into complete ADC words in order to get the bits off the calorimeter faster. There are two data lines, TEM_DAT0 and TEM_DAT1 for sending data to the TEM. TEM_DAT0 is used for both command read data and ADC data. TEM_DAT1 is used only for ADC data. Thus the two data lines get the ADC data off the calorimeter board quicker.

The data lines are implemented with LVDS, asserted low levels.



6.6 Trigger Encoding

Trigger requests to the TEM are on the L1_TREQ_HE and L1_TREQ_LE lines. The signalling format is minimum pulse width of 200 nsec, and maximum pulse length is time-over-threshold. The trigger communication lines between the GCRC and TEM are LVDS, asserted low.

6.7 Front-End Trigger Processing

The High Energy and Low Energy Wired-OR triggers from the GCFE chips are sampled on the edge of the system clock.

6.8 Operational Parameter Registers

Table 2 shows the address space reserved for the GCRC function bit mapping: The first bit of the 5 bit function field indicates read, bit “1”, or write, bit “0”. The definition of the GCRC configuration register is shown in Table 3

Table 2. Command Function Bit Definitions

Funcion Bits (5 bit binary)	Definition
00000	Write not used
00001	Write Reset GCRC
01000	Write GCFE Configuration Register
11000	Read GCFE Configuration Register
01001	Write Time Delay 1, Peak Hold to ADC Acquisition
11001	Read Time Delay 1, Peak Hold to ADC Acquisition
01010	Write Time Delay 2, ADC Acquisition time
11010	Read Time Delay 2, ADC Acquisition time
01011	Write Time Delay 3, ADC Conversion time
11011	Read Time Delay 3, ADC Conversion time
01100	Write Digital to Analog Converter (DAC) setting
11100	Read Digital to Analog Converter (DAC) setting
10000	Read Status Register
10001	Read 16 bits of Last Command Error

Table 3. GCRC Configuration Register Bit Definition

Bit	Definition
0 LSB	GCRC Parity, 0 Odd Parity, 1 Even Parity
1	ADC Conversion Mode, 0 internal clock, 1 external clock
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	

7 Pin Names

Table 4. Input Pin Definitions

DAT0_P to DAT11_P	Data from GCFE chips, Positive LVDS
DAT0_N to DAT11_N	Data from GCFE chips, Negative LVDS
TEM_CMD_P	Command from TEM, Positive LVDS
TEM_CMD_N	Command from TEM, Negative LVDS
TEM_CLK_P	System Clock from TEM, Positive LVDS
TEM_CLK_N	System Clock from TEM, Negative LVDS
HE_DISC_P	GCFE “Wired-OR” High Energy layer trigger, Pos LVDS
HE_DISC_N	GCFE “Wired-OR” High Energy layer trigger, Neg LVDS
LE_DISC_P	GCFE “Wired-OR” Low Energy layer trigger, Pos LVDS
LE_DISC_N	GCFE “Wired-OR” Low Energy layer trigger, Neg LVDS
ADC_DAT0 to ADC_DAT11	ADC Data from each Log End
TEM_RESET_P	Reset from TEM, Positive LVDS
TEM_RESET_N	Reset from TEM, Negative LVDS
ADDR0 to ADDR3	Hard-Wired GCRC Address, Bits 0,1,2,3

Table 5. Output Pin Definitions

DAQ_CLK_P	Clock to GCFE chips, Positive LVDS
DAQ_CLK_N	Clock to GCFE chips, Negative LVDS
CMD_P	Command to GCFE chips, Positive LVDS
CMD_N	Command to GCFE chips, Negative LVDS
RESET_P	Reset to GCFE chips, Positive LVDS
RESET_N	Reset to GCFE chips, Negative LVDS
L1_TREQ_HE_P	L1 Trigger Request, High Energy, Positive LVDS
L1_TREQ_HE_N	L1 Trigger Request, High Energy, Negative LVDS
L1_TREQ_LE_P	L1 Trigger Request, Low Energy, Positive LVDS
L1_TREQ_LE_N	L1 Trigger Request, Low Energy, Negative LVDS
START_ACQ_P	GCFE Start Acquisition Cycle, Positive LVDS
START_ACQ_N	GCFE Start Acquisition Cycle, Negative LVDS
ADC_CS\	ADC Chip Select
ADC_CLK	ADC Clock
DAC_CS\	Calibration DAC Chip Select
DAC_CLK	Calibration DAC Clock
DAC_DATA	Calibration DAC Data
TEM_DAT0_P	Data to TEM, “Pipe” 0, Positive LVDS
TEM_DAT0_N	Data to TEM, “Pipe” 0, Negative LVDS
TEM_DAT1_P	Data to TEM, “Pipe” 1, Positive LVDS
TEM_DAT1_N	Data to TEM, “Pipe” 1, Negative LVDS

Table 6. Power Pin Definitions

DVDD	Digital VDD, moninally 3.3 Volts
DGND	Digital ground

8 Pin Numbers

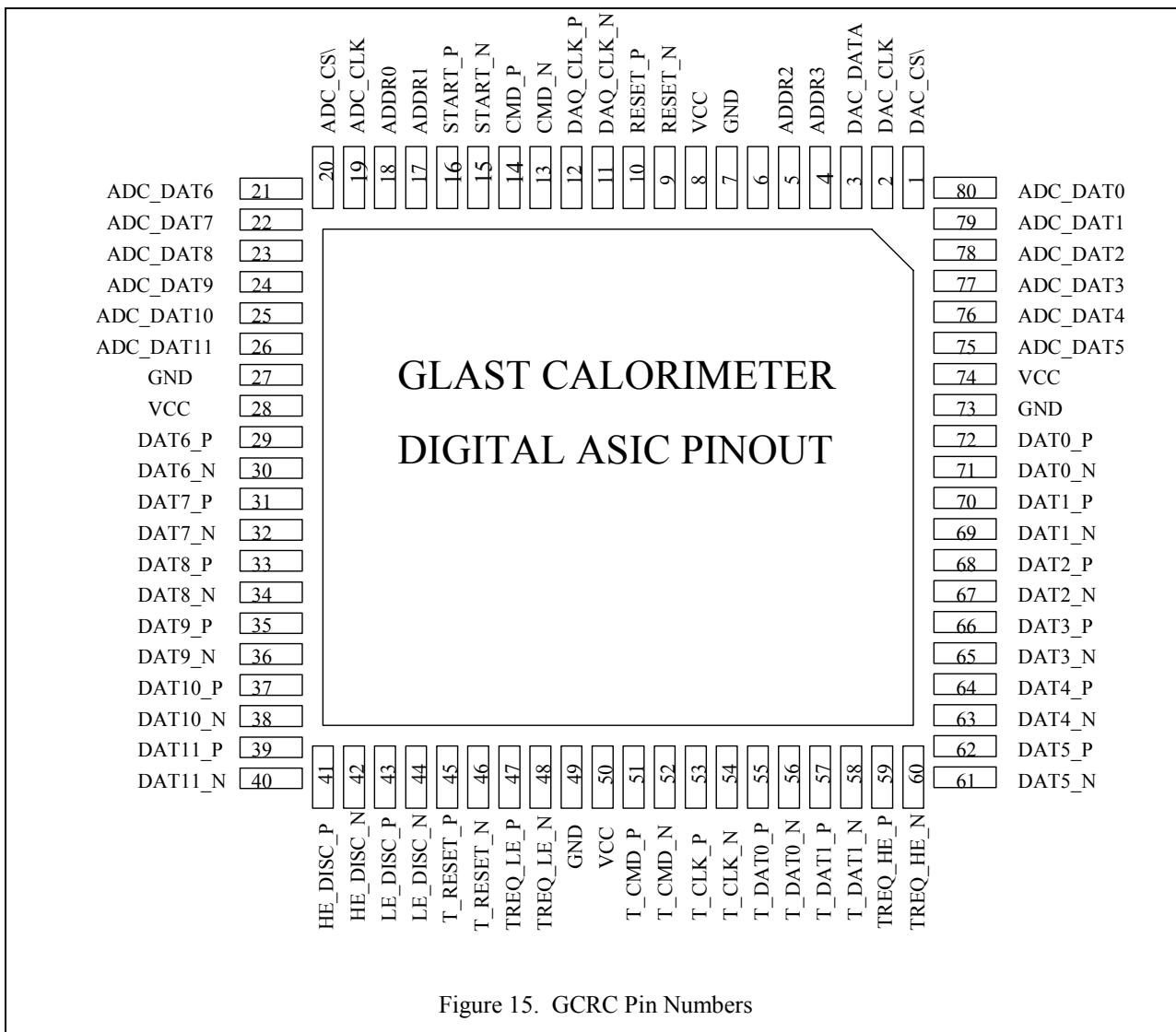


Figure 15. GCRC Pin Numbers

Figure 15 shows the pin assignments for the GCRC ASIC mounted in a 80 pin TQFP package.